REMARKS

Claims 1-17 are pending in the present application. Three paragraphs of the specification have been amended to correct several minor errors.

Applicants respectfully request reconsideration of the application in view of the foregoing amendments and the remarks appearing below.

Rejections Under 35 U.S.C. § 102

The Examiner has rejected claims 1, 3-6, 8, and 15-17 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,181,144 to Hembree et al., stating Hembree et al. disclose all the elements of these claims. Applicants respectfully disagree.

Hembree et al. disclose a semiconductor probe card (20) that includes a plurality of probe contacts (22), each for contacting a corresponding one of a plurality of wafer contacts (14) located on die (12) of a semiconductor wafer (10). The probe contacts 22 are provided for performing various tests on the circuitry onboard the die, including measuring the resistance between two wafer contacts. The probe contacts 22 are in electrical communication with a suitable tester (26) configured for the particular tests performed on the die. The Hembree et al. probe card includes only one contact 22 for each wafer contact 14.

Referring to FIGS. 6A and 6B of the Hembree et al. patent, one test performed using the Hembree et al. probe card measures the resistance of internal traces (88) between two of the wafer contacts, in particular, wafer contacts 14Vcc-1 and 14Vcc-2. This is accomplished by contacting probe contact 22-1 with wafer contact 14Vcc-1 and probe contact 22-2 with wafer contact 14Vcc-2 and performing the various steps of the test.

In contradistinction, the present invention is directed to a system for, and method of, testing the resistance of each probe pad of a device under test that includes contacting two probes to each probe pad. One of the probes is a forcing probe that applies an electrical signal to the probe pad, and the other probe is a sensing probe for sensing the electrical signal applied by the forcing probe.

Regarding independent claim 1, this claim requires a forcing probe and a sensing probe, each for contacting a single probe pad simultaneously with the other during the test. Hembree et al. disclose a plurality of wafer contacts 14, each contacted by only one probe contact 14 at any one time during the test. That is, Hembree et al. are completely silent on providing two probes

for contacting a single probe pad simultaneously with one another, as claim 1 requires. In addition, Hembree et al. do not disclose a variable power supply in electrical communication with the first and second probes for varying the first signal based upon the second signal, as claim 1 also requires. Since Hembree et al. do not disclose at least these features of independent claim 1, the Hembree et al. patent cannot anticipate this claim, nor claims 2-8 that depend therefrom.

Regarding independent claim 9, this claim requires applying a first electrical signal to a probe pad, sensing a second electrical signal at that same probe pad, and adjusting the first electrical signal based upon the second electrical signal. As discussed above, Hembree et al. do not disclose contacting two probe contacts 22 with a single wafer contact 14 simultaneously with one another. Therefore, Hembree et al. cannot disclose the "dual-probe" method of claim 9, which includes applying a first electrical signal to, and sensing a second electrical signal from, a single probe pad and adjusting the first signal based on the second signal. Since Hembree et al. do not disclose these elements of independent claim 9, the Hembree et al. patent cannot anticipate this claim, nor claims 10-17 that depend therefrom.

For at least the foregoing reasons, Applicants assert the anticipation rejection of claims 1, 3-6, 8, and 15-17 in view of the Hembree et al. patent is improper. Accordingly, Applicants respectfully request that the Examiner withdraw this rejection.

Rejections Under 35 U.S.C. § 103

The Examiner has rejected claims 2, 10-12, and 14 under 35 U.S.C. § 103 as being obvious in view of Hembree et al. patent, discussed above, stating Hembree et al. disclose a system and method each having all of the elements of these claims, except for (1) a plurality of forcing and sensing probes, (2) measuring a third electrical signal at a second probe, and (3) a feedback controller. The Examiner then asserts it would have been obvious to a person having ordinary skill in the art at the time of the invention to provide the Hembree et al. system and method with the missing elements mentioned above in view of design choice. Applicants respectfully disagree.

As discussed above in connection with the anticipation rejection with respect to the Hembree et al. patent, Hembree et al. do not provide the basis teaching of a dual-probe technique wherein two probes contact a single probe pad simultaneously with each other. Therefore, the

asserted combination of the Hembree et al. patent and design choice would lack the dual-probe features of the present claims discussed above in connection with the anticipation rejection. In addition, the features of independent claims 1 and 9 missing from the Hembree et al. disclosure are not disclosed or suggested in any of the references of record. Moreover, these features are not obvious in view of the references of record, alone or in combination with one another, by virtue of design choice, or otherwise.

For at least the foregoing reasons, Applicants believe the present obviousness-type rejection of claims 2, 10-12, and 14 in view of the Hembree et al. patent is improper. Therefore, Applicants respectfully request that the Examiner withdraw this rejection.

The Examiner has rejected claims 7 and 13 under 35 U.S.C. § 103 as being obvious in view of Hembree et al. patent, discussed above, and U.S. Patent No. 4,038,599 to Bove et al., stating Hembree et al. disclose a system and method each having all of the elements of these claims except a plurality of forcing probes and a matrix switch. The Examiner then asserts it would have been obvious to a person having ordinary skill in the art at the time of the present invention to combine the Hembree et al. and Bove et al. teachings to provide the elements of claims 7 and 13 missing from the Hembree et al. system and method. Applicants respectfully disagree.

Bove et al. disclose a high density wafer contacting and testing system. The system includes a probe assembly (20) having a plurality of probes (19), each for contacting a corresponding one of a plurality of test pads (16a) located on a device under test.

Again, as discussed above in connection with the anticipation rejection in view of the Hembree et al. patent, Hembree et al. do not provide the basic teaching of a dual-probe technique wherein two probes contact a single probe pad simultaneously with one another. Bove et al. similarly do not teach a dual-probe technique. Therefore, the asserted combination of the Hembree et al. and Bove et al. patents would lack the dual-probe features of the present claims discussed above relative to the anticipation rejection. In addition, the features of these claims missing from the Hembree et al. and Bove et al. disclosures are not disclosed or suggested in any of the other references of record. Moreover, these features are not obvious in view of the references of record, alone or in combination with one another, by virtue of design choice, or otherwise.

For at least the foregoing reasons, Applicants believe the present obviousness-type rejection of claims 7 and 13 in view of the Hembree et al. and Bove et al. patents is improper. Therefore, Applicants respectfully request that the Examiner withdraw this rejection.

Other Reference Cited by the Examiner

Further, Applicants have reviewed the additional reference cited by the Examiner, i.e., U.S. Patent No. 4,423,373 to LeCroy, Jr., and respectfully submit that LeCroy, Jr. does not disclose or suggest the subject matter of the present claims.

CONCLUSION

In view of the foregoing, Applicants submit that claims 1-17 are in condition for allowance. Therefore, prompt issuance of a Notice of Allowance is respectfully solicited. If any issues remain, the Examiner is encouraged to call the undersigned attorney at the number listed below.

Respectfully submitted,

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Attachment:
Substitute Paragraph Showing Amendments

SUBSTITUTE PARAGRAPH SHOWING AMENDMENTS

As manufacturers continually reduce the size of microelectronic devices contained in very large scale integration (VLSI) integrated circuits (ICs), it is becoming more difficult to test these devices to determine whether or not they function properly. This is so because as the size of the devices decreases, the electrical resistance through these devices also [decrease] decreases. Therefore, the sensitivity of the test measurements, and, relatedly, accuracy of the electrical signals reaching the devices during testing, must increase accordingly.

However, the use of copper-based metallurgy in microelectronic devices increases the difficulty of providing the devices with an accurate signal. Unlike test [connection] connections made to the aluminum probe pads of microelectronic devices having aluminum-based metallurgy, test connections made to copper probe pads are problematic due to the formation of layers of copper oxide on the probe pads and the test probes. These copper oxide layers increase the contact resistance between the test probes and probe pads, decreasing the voltage applied across the devices. The reduction in voltage decreases the accuracy and sensitivity of the measurements made during testing and often leads to false failure determinations.

The resistance caused by the layers of copper oxide and other materials is commonly referred to as "contamination resistance." Various systems and methods have been developed for measuring contamination resistance. For example, Japanese Publication No. 11-133075 is directed to a system for and method of determining whether or not the contamination resistance of one or more probe pads is too large to obtain useful measurement data from a device under test (DUT). The system comprises a probe card having a plurality of probes, or needles, for testing a [device under test (]DUT[)] having a plurality of probe pads. The probe card provides a pair of probes for contacting each probe pad of the DUT. The pair of probes associated with each probe pad are spaced from one another and contact the corresponding probe pad at different locations.